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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,401	07/22/2002	Yoshifumi Nagai	2002-0386A	2955

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EXAMINER	
LESPERANCE, JEAN E	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/088,401	NAGAI ET AL.	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,24-26 and 31* is/are allowed.

6)☒ Claim(s) *1, 3, 7-9,12-23, 27-30, and 32* is/are rejected.

7)☒ Claim(s) *4-6,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 to 32 are presented for examination.

2. The rejection 112-second paragraph of claims 1-12 is withdrawn.

3. The objection is claim 1 is withdrawn.

4. The allowable subject matter of claims 13-23, 27-30 and 32 is withdrawn.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 7-9,12-23, 27-30, and 32 are rejected under 35 USC 102 (b) as being unpatentable over US Patent # 5,815,136 ("Ikeda et al.").

As to claims 1,13, 15, 19, 27-30 and 32, Ikeda et al. teach the liquid crystal panel Fig.19 (1807) corresponding to a display section; the scanning circuit Fig.19 (1805) corresponding to a vertical driving section; the data driver Fig.19 (105) corresponding to a plurality of horizontal driving section; the CPU (1601) inherently includes an I/O section for communication and a timing control section for controlling corresponding to a driving control section; I/O (1603) in cooperation with the CPU (1601) corresponding to a first communication section; the timing controller Fig.19 (1904) in cooperation with the CPU (1601) corresponding a second communicating section; the output voltage

lines Fig.19 (127) corresponding to each of the horizontal driving sections has a horizontal communicating section; driver ID's generated by the driver ID generators Fig.29A (96) and Fig.29B (97) are characteristic data for informing mounted liquid crystal drivers of their arrangement positions corresponding to individual identification information to discriminate the horizontal driving sections; each data in the timing controller inherently is formatted in a predetermined format and the liquid crystal panel is on Fig.19 ((1807), the CPU can access the plurality of liquid crystal drivers 105 individually in such a manner that whether or not the access from the CPU is an access to each liquid crystal driver itself is judged from the address mode signal line and an inputted address to generate a chip selection signal in that liquid crystal driver. In the case of the liquid crystal display system of FIG. 29 or 30, the address mode signal 150 of the driver 105-1 is set to be MODEA2, A1, A0="000" (driver ID=0) and the address mode signal 151 of the driver 105-2 is set to be MODEA2, A1, A0="010" (driver ID=2). Thereby, for example, when an address "0EF27H" is designated from the CPU 701, the liquid crystal driver 105-1 internally generates a chip selection signal and the access is performed. When an address "0EF28H" is designated from the CPU 701, the liquid crystal driver 105-2 internally generates a chip selection signal and the access is performed (See Figures 33, 34, and 35); memory cell (2425) corresponding to information storing section and figure 33 corresponding to different data packets.

As to claims 3, 14 and 20, Ikeda et al. teach each of said driver circuit elements includes selecting means for receiving driver identification information indicative of the arrangement position of that driver circuit element from the exterior and judging,

whether or not an address given from said external device is an address for access to that driver circuit element itself, on the basis of said driver identification information to generate a selection signal which selects the display memory in that driver circuit element (column 42, lines 50-58) corresponding to each of the horizontal driving sections stores a common ID to be received commonly for all of the horizontal sections.

As to claim 7, Ikeda et al. teach the driver data Fig.19 (125) corresponding to the horizontal driving section and the output data 127 from the data driver lines are connected serially to the timing controller.

As to claim 8, Ikeda et al. teach the alternating current signal is supplied from outside of the driver. Numeral 197 denotes an oscillator for generating a reference clock signal for display, numeral 198 the reference clock signal for display, and numeral 130 the scanning circuit which generates a scanning signal 131 and the display synchronizing signal 104 for liquid crystal driver. Numeral 131 denotes a bus of the scanning signal generated by the scanning circuit 130, and numeral 132 a liquid crystal panel having a resolving power of 320 (dots).times.240 (lines) (column 37-46).

As to claim 9, Ikeda et al. teach a numeral 2435 an FRC selector for selecting output data from the FRC data bus 2434 and the data bus 2432, numeral 2436 a data bus of 160 bits, numeral 2437 a 160-bit latch circuit for simultaneously latching data of 160 bits of the data bus 2436 when the latch signal 2430 takes a high level, numeral 2438 a data bus of output data from the latch circuit 2437, numeral 2439 a 160-bit latch circuit for simultaneously latching data of 160 bits on the data bus 2438 by virtue of a

rising edge of the latch signal 2431, numeral 2440 a data bus of output data from the latch circuit 2439, numeral 2441 a level shifter for shifting a signal voltage to a voltage level corresponding to a liquid crystal driving voltage, numeral 2442 a data bus of the level-shifted data, numeral 2443 a decoder for decoding an alternating current signal and data, numeral 2444 a bus of a decoded selection signal, numeral 2445 a voltage selector for selecting a liquid crystal applied voltage, and numeral 2446 an output voltage line. Numeral 2447 denotes an oscillator for generating a reference clock signal for display, numeral 2448 the reference clock signal for display, and numeral 2449 the scanning circuit (see figure 47A).

As to claim 12, Ikeda et al. teach a liquid crystal panel Fig.19 (1807), which inherently includes a substrate integrated with the pixel elements where the light elements and the driving circuit board having driving circuits driving the lighting elements and wherein the driving circuits are disposed between the lighting elements.

As to claims 16-18, Ikeda et al. teach the liquid crystal driver 2405 is inputted with a 3-bit control signal including address mode signals MODEA2, MODEA1 and MODEA0 (see FIG. 33) determined in accordance with the arrangement position of the liquid crystal driver. By decoding this control signal, it is possible to set eight driver ID's of ID0 to ID7. FIGS. 51, 52, 53 and 54 show the configuration of liquid crystal drivers and address ID's in the cases where the resolving power of the liquid crystal panel is 240 (horizontal).times.160 (vertical), 240 (horizontal).times.320 (vertical), 480 (horizontal).times.320 (vertical), and 480 (horizontal).times.640 (vertical), respectively. In the case of the liquid crystal display system of FIG. 47 or 48, the address mode

signal line 2406 of the driver 2405-1 is set to be MODEA2, A1, A0="000" (driver ID=0) and the address mode signal line 2407 of the driver 2405-2 is set to be MODEA2, A1, A0="010" (driver ID=2). Namely, a change-over to an address control corresponding to the liquid crystal arrangement position of the liquid crystal driver is made by the setting of the address mode signal line, thereby enabling correct address designation for the memory cell 2425 (see Figure 47A).

As to claims 21-23, Ikeda et al. teach a liquid crystal panel Fig.19 (1807) corresponding to the lighting elements, the control data is image data for image-displaying and the control data is illuminating data for an illumination.

Allowable Subject Matter

6. Claims 4, 5, 6, 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2, 24, 25,26, and 31 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: the claimed invention is directed to a display apparatus. Independent claims 2, 24-26 and 31 identify a uniquely distinct feature " a data packets having a control field Fig.4 (21), a control identification information Fig.4 (24) and an information field Fig.4 (22). Dependent claim 4 identifies a uniquely distinct feature "each of the horizontal driving communicating sections has receiving section Fig.6 (28), output selecting circuit (30) and outputs a control field (21) of an input data packet (20)". Dependent claim 5

identifies a uniquely distinct feature "each of the horizontal driving communicating sections has a disturbance data retaining section (29), a control field (22) of the disturbance data reading packet (20B)". Dependent claim 6 identifies a uniquely distinct feature "each of the horizontal driving communicating sections has a data reversing section Fig.11 (38) reversing of the information field (22)". The closest art, Ikeda et al. as discussed above, either singularly or in combination, fails to anticipate or render the above limitations obvious.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703) 308-6413. The examiner can normally be reached on from Monday to Friday between 8:OOAM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709 .

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Date 1/8/2005

Art unit 2674

HENRY N. TRAN
PRIMARY EXAMINER